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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,418	07/29/2003	Masayoshi Noguchi	7217/69608	6003

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EXAMINER	
TU, JULIA P	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,418	NOGUCHI ET AL.	
	Examiner	Art Unit	
	Julia P. Tu	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8 and 10-13* is/are rejected.

7)☒ Claim(s) *4 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: an adder 31 on the last line of page 13 and a shift computing element 32 on the first line of page 14 are not shown in the drawing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 10-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are generally narrative and indefinite,

failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (5,859,603) in view of Adachi et al. (US 2002/0186440).

(1) with regard to claim 1:

As shown in figure 1, Noguchi et al. disclose digital signals are subjected to predetermined processing (see figure 1; note 1 bit digital signal pass through bit length converter), a processed digital signal having signal amplitude values exceeding signal amplitude values of the digital signals is inputted (figure 1, note: a processed digital signal is the signal coming out of the bit length converter; it is obvious that after going through the bit length converter, the processed signal have larger amplitude than the 1 bit digital signal (i.e. input signal)); the processed signals go through sigma delta modulator with a quantizer (block 9 in figure 1), and the quantized amplitude values equal to the signal amplitude values of digital signals (figure 1, note the output of 1-bit quantizer 25 is 1 bit digital signal which is equal to the input signal).

Noguchi et al. disclose all of the subject matter above except for the first and second delta sigma modulating means.

However, Adachi et al. disclose a digital signal processing device comprising first delta sigma modulating means (block 200 in figure 6) including first quantizing means (block 202 in figure 6) having quantized amplitude values allowing at least quantization of signal amplitude of the inputted processed digital signal; and second delta sigma modulating means (block 220 in figure 6) including second quantizing means (block 222 in figure 6).

It is desirable to have the first and second delta sigma modulating means to modulate digital signals in order to provide a transmitting circuit apparatus having good linearity, high transmission output power efficiency, and small power consumption (page 1, paragraph [0019]). Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to include the first and second delta sigma modulating means as taught by Adachi et al to the system as taught by Noguchi et al. to provide a transmitting circuit apparatus having good linearity, high transmission output power efficiency, and small power consumption (page 1, paragraph [0019]).

(2) with regard to claim 2:

Adachi et al. further disclose the second delta sigma modulating means further includes delaying means for delaying a part of a quantized signal outputted from the first quantizing means and outputting the delayed part to the second quantizing means (see block 221 in figure 6, note it is obvious that the signal would be delayed before entering the second quantizer 222) when quantized data outputted from the first quantizing

means has an amplitude value exceeding the quantized amplitude values of the second quantizing means (figure 6, page 7, paragraph [0125]; note that the signal coming to the second quantizer has been subtracted at block 210; therefore, it is obvious that the quantized data outputted from the first quantizing means (block 202 in figure 6) has the an amplitude value exceeding the quantized amplitude values of the second quantizing means (block 222 in figure 2).

(3) with regard to claim 5:

However, Noguchi et al. further disclose the quantizing means convert a delta sigma modulated output of the delta sigma modulating means to one bit (column 5, lines 11-14).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Noguchi et al. (5,859,603).

As shown in figure 1, Noguchi et al. disclose digital signals are subjected to predetermined processing (see figure 1; note 1 bit digital signal pass through bit length converter), a processed digital signal having signal amplitude values exceeding signal amplitude values of the digital signals is inputted (figure 1, note: a processed digital signal is the signal coming out of the bit length converter; it is obvious that after going

through the bit length converter, the processed signal have larger amplitude than the 1 bit digital signal (i.e. input signal)); the processed signals go through sigma delta modulator with a quantizer (block 9 in figure 1), and the quantized amplitude values equal to the signal amplitude values of digital signals (figure 1, note the output of 1-bit quantizer 25 is 1 bit digital signal which is equal to the input signal).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (5,859,603) in view of Adachi et al. (US 2002/0186440).

Noguchi et al. disclose all of the subject matters in claim 6 above except for a step of delaying processing for quantizing a part where a quantized value of the quantized modulated signal exceeds the signal amplitude values of the digital signals.

However, Adachi et al. disclose a cascade of two delta sigma modulators with a step of delaying processing for quantizing a part where a quantized value of the quantized modulated signal exceeds the signal amplitude values of the digital signals (see block 221 in figure 6, note it is obvious that the signal would be delayed before entering the second quantizer 222; figure 6, page 7, paragraph [0125]; note that the signal coming to the second quantizer has been subtracted at block 210; therefore, it is obvious that the quantized data outputted from the first quantizing means (block 202 in figure 6) has the an amplitude value exceeding the quantized amplitude values of the second quantizing means (block 222 in figure 2).

It is desirable to include a cascade of two delta sigma modulators with a step of delaying processing for quantizing a part where a quantized value of the quantized

modulated signal exceeds the signal amplitude values of the digital signals to provide a transmitting circuit apparatus having good linearity, high transmission output power efficiency, and small power consumption (page 1, paragraph [0019]). Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to include a step of delaying processing for quantizing a part where a quantized value of the quantized modulated signal exceeds the signal amplitude values of the digital signals as taught by Adachi et al. to the method as taught by Noguchi et al. so as to provide a transmitting circuit apparatus having good linearity, high transmission output power efficiency, and small power consumption (page 1, paragraph [0019]).

9. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi et al. (US 2002/0186440) in view of Yu (US 6,518,899).

(1) with regard to claim 3:

Adachi et al. disclose all of the subject matter in claim 1 above except for the quantizing means of the delta sigma modulating means performs quantization with quantized values each comprising n bits (n=2 or more), and uses two values having zero interposed between the two values and separated from the two values by equal quantities and values having a difference equal to a difference between the two values as the quantized values.

However, Yu teach for the quantizing means of the delta sigma modulating means performs quantization with quantized values each comprising n bits (n is 2 or more), and uses two values having zero interposed between the two values and

separated from the two values by equal quantities and values having a difference equal to a difference between the two values as the quantized values (column 6, lines 11-19).

It is desirable to include for the quantizing means of the delta sigma modulating means performs quantization with quantized values each comprising n bits (n=2 or more), and uses two values having zero interposed between the two values and separated from the two values by equal quantities and values having a difference equal to a difference between the two values as the quantized values so that the modulator intends to be more stable with more levels of quantization (column 2, lines 8-10). Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to include the system as taught by Yu to the system as taught by Adachi et al. to improve data rates, noise reduction, linearity and accuracy (column 1, lines 29-30).

(2) with regard to claim 8:

Adachi et al. disclose all of the subject matter in claim 6 above except for the delta sigma modulated signal obtained by subjecting the inputted processed signal to delta sigma modulation is quantized by n bits (n is 2 or more), and two values having a zero interposed between the two values and separated from the two values by equal quantities and values having a difference equal to a difference between the two values are used as quantized values.

However, Yu teach for the delta sigma modulated signal obtained by subjecting the inputted processed signal to delta sigma modulation is quantized by n bits (n is 2 or more), and two values having a zero interposed between the two values and separated

from the two values by equal quantities and values having a difference equal to a difference between the two values are used as quantized values (column 6, lines 11-19).

It is desirable to include for the delta sigma modulated signal obtained by subjecting the inputted processed signal to delta sigma modulation is quantized by n bits (n is 2 or more), and two values having a zero interposed between the two values and separated from the two values by equal quantities and values having a difference equal to a difference between the two values are used as quantized values so that the modulator intends to be more stable with more levels of quantization (column 2, lines 8-10). Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to include the method as taught by Yu to the method as taught by Adachi et al. to improve data rates, noise reduction, linearity and accuracy (column 1, lines 29-30).

Allowable Subject Matter

10. Claims 4 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter. Claims 4 and 9 disclose the quantizing means of the delta sigma modulating means uses values equal to two least significant quantized values of the quantized values of the quantizing means as quantized values. Adachi et al. (US 2002/0186440),

Noguchi et al. (5,859,603), and Yu (US 6,518,899) fail to teach the quantizing means of the delta sigma modulating means uses values equal to two least significant quantized values of the quantized values of the quantizing means as quantized values. The distinct features have been added to the independent claims 4 and 9, therefore, rendering them allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julia P. Tu whose telephone number is 571-270-1087. The examiner can normally be reached on 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

J.T.
10-28-2006

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER